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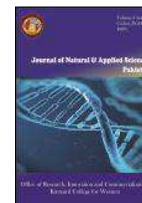

ANALYSIS OF ON-RESISTANCE IN NORMALLY-OFF 4H-SiC VERTICAL. JUNCTION FIELD EFFECT TRANSISTOR

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Abstract
2D numerical simulation of normally-off 4H-SiC VJFET (Vertical Junction Field Effect Transistor) is performed by varying different parameters including temperature (300-600 K), channel width (0.85 µm, 1.05 µm and 1.25 µm) and gate voltage using TCAD (Technology Computer Aided Design) numerical simulator. Main concern is the reliability of SiC VJFET under high temperature and high electric field. In this report, we focus on temperature dependent output characteristics with different channel widths and gate voltages. In forward characteristic mode, excellent temperature behavior is observed, and simulation results show that the forward current increases from 1.14 A (300 K) to 5.43 A (600 K) at channel width 1.25 µm with gate voltage 3.0 V. We have observed that the forward current increases with the increase of channel width and the gate voltage influences forward saturation current. We report the specific on-resistance of 2.012 mΩ.cm^2, based on 10 µm drift layer, doped to 7 x 10^{15} cm^3.Under varying gate voltages and temperatures, unipolar and bipolar mode of operation is studied. The leakage current is observed in the range of nA at temperature 300 K and increases in the range of µA at temperature 600 K. A high value of 751 MW/cm^2 for the figure of merit (FOM = V_B^2/R_{sp-on}) is achieved.

1. Introduction

Everyday life has benefitted through the technology revolutions. The development of semiconductor devices has become a major strength in this revolution which has led to incredible progress of society. Since 1950s, silicon-based power devices have been extensively used in power electronic systems. Because dealing with the power devices, Si based devices have limitations regarding,

- operating temperature,
- breakdown voltage,
- specific on-resistance,
- thermal conductivity,
- leakage currents, and
- power dissipation.

Due to the above-mentioned limitations of Si material properties, a new material for power devices had been required. Silicon Carbide (SiC) has gained significant consideration as favorable material with the potential of replacing Si in the fabrication of power devices [1]. The unipolar SiC devices are suitable for applications regarding high voltage due to considerable high mobility of electrons and high value of electric field strength. SiC JFETs do not suffer from bipolar instability. These devices had offered an efficiency of around 99 % [2].

This resulted in the reduction of the size, weight and cost of these structures. SiC based power devices propose great technological improvements and can work in severe environmental conditions. Power devices based on silicon carbide (SiC) had the prospective to enhance the energy efficiency due to the appropriate properties of the material.

In 1891, Edward G. Acheson accidently discovered SiC. His target was the synthesis of artificial diamonds. In an iron bowl, the mixture of clay and coke (powdered) was heated by electric current. Green bright crystals were attached to electrode of carbon. Initially it was considered as a new compound of carbon and alumina. The compound was named “Carborundum” after the natural mineral form of alumina [5]. About the same period, Henri Moissan of France prepared the same compound by the mixture of carbon and quartz. This product held the name “Moissanite”, that was the mineralogical term [6].

SiC is considered as the hardest synthetic material. In Mohs, its hardness rating is 9 which is equivalent to diamond. It has high thermal conductivity, low thermal expansion and resistant to chemical reaction. It is classified as “semiconductor” [10].

Silicon. Carbide Properties are;

- ✓ Low. density
- ✓ High. strength
- ✓ Low thermal. expansion
- ✓ High thermal. conductivity
- ✓ High. hardness
- ✓ High. elastic modulus
- ✓ Excellent thermal. shock resistance
- ✓ Superior chemical. inertness
- ✓ High radiation stability

Silicon Carbide (SiC) is the most feasible material for high temperature and high power devices because of its wide band gap. The operating temperature of SiC devices is 6-7 times higher than those of Si devices. High critical electric field (E_C), i.e. around 2.2 x 10^6 V/cm is due to the large band-gap. This lowers the on-state resistance (R_{on}), which in turn lowers the power dissipation during the on-state. The drawback is low electron mobility and manufacturing difficulty of SiC.

Due to shortcoming of 3C-SiC, most power structures are fabricated using either 4H-SiC or 6H-SiC types. Among 4H-SiC and 6H-SiC types, 4H-SiC has high carrier mobility and low intrinsic carrier concentration, also it is readily available.

Table 1.1: Fundamental material properties of SiC and other semi-cond. at 300 K

Material Property	**Si**	**GaAs**	**GaN**	**3C-SiC**	**4H-SiC**	**6H-SiC**
Crystal. Structure	Diamond	Zincblende	Hexagonal	Cubic	Hexagonal	Hexagonal
Band gap, Eg (eV)	1.12	1.43	3.4	2.36	3.26	3.0
Breakdown field, [ND=1017cm-3] EB(MV/cm)	0.6	0.65	3.5	1.5	3.5	3.5
Saturated Drift Velocity, VD(cm/s)	1x107	1x107	2.5x107	2.5x107	2x107	2x107
Electron mobility, µn(cm2/V-s)	1350	8500	1000	1000	950	500
Hole mobility, µp (cm2/V-s)	480	400	30	40	120	80
Critical field, EC (V/cm)	2.5x105	3x105	3x106	2x106	2.2x106	2.5x106
Thermal Conductivity, λ (W/cm K)	1.5	0.46	1.3	5.0	4.9	4.9
Maximum operating temperature (oC)	150	460	750	600	1000	800
Relative Dielectric Constant, εr	11.9	13.0	9.5	9.7	10	10

The energy band gap (E_G) in 4H-SiC as a function of temperature is approximated by the equation 1.1,

$$E_G = 3.265 - 6.5 \text{ x } 10^{-4}\left(\frac{T^2}{T+1300}\right) \quad (1.1)$$

Regarding practical use of JFET, there are two modes of operation for JFETs;
1) Enhancement-mode, (known as normally-off devices)
2) Depletion-mode, (known as normally-on devices
In normally-off structure, a positive gate bias is needed to turn-on the device because in normally-off state, the conducting channel width
(W_C) is reduced due to the formation of depletion region by gate terminals [17]. For normally-on devices, no gate voltage is required to turn-on the device and to turn-off the device, a negative gate voltage is required. The enhancement-mode or normally-off structure blocks high drain to source voltage at zero gate bias voltage while the depletion-mode or normally-on structure, there is high drain current even at zero gate bias voltage. Normally-on devices can conduct high current density and able to offer low specific-on resistance as compare to normally-off devices. Normally-on devices are not suitable for applications, where the power is supplied at the start up. In such cases normally-off devices are preferred, e.g. in low power drives and power supplies. A normally-on device is not wanted for power electronics because it needs additional protection circuitry to protect a dc bus short if the gate signal fails. Normally-off VJFET is preferable because it gives safety to high power systems without failure [18]. For high power and high temperature applications, the development of normally-off VJFETs is necessary. TI-VJFET using 4H- SiC as normally-off device was first demonstrated in 2003.The recent advancement in device fabrication is the use of simulation techniques. Simulation technology is primarily employed during the growth of a new structure or device. Simulation process supports the entire progress cycle, from initial concept development to design, fabrication, testing and optimization.

The best software which is able to design and characterize the semiconductor materials and devices is TCAD (Technology Computer Aided Design). It comprises of a set of tools which are developed for simulation and optimization of semiconductor devices. These tools provide a tactical sense to innovation.

Table 1.2: History of development of TCAD

Year	Institute	Process	Device
1977	R.W.Dutton, Stanford U.	SUPREM-I (1D)	PISCES
1979	Technology Modeling Associates (TMA)	TSUPREM 4 (2D)	MEDICI
1989	Silvaco International	ATHENA (2D)	ATLAS
1989	Integrated Systems E ngineering (ISE)	DIOS (2D)	DESSIS
1992	TMA	TAURUS (3D) TSUPREM 4	MEDICI
1993	M.Law, Florida U.	FLOOPS (3D)	-
2002	ISE	FLOOPS (3D)	-
2005	Synopsys	SENTAURUS (3D TAURUS)	3D TAURU S

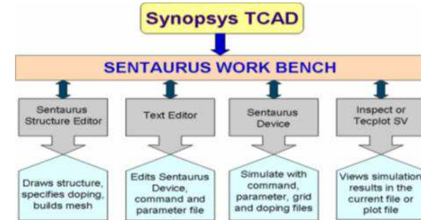


Figure 1.1: Tool Flow For Sentaurus Workbench

2. Device Model Approach

2.1 Low Field. Mobility Model

The temperature dependent. and low electric field doping level electron mobility (μ_n) and hole mobility (μ_p) can be modeled by Caughey-Thomas equation;

$$\mu_n = \frac{\mu_{max,n} * (\frac{T}{300})^{-\alpha_n}}{1+\left(\frac{N_i}{N_{ref,n}}\right)^{\gamma_n}} \quad (2.1)$$

$$\mu_p = \mu_{min} + \frac{\mu_{max,p} * (\frac{T}{300})^{-\alpha_p}}{1+\left(\frac{N_i}{N_{ref,p}}\right)^{\gamma_p}} \quad (2.2)$$

where,

μ_{min}, α, and γ are theCaughey-Thomas parameters.

2.2 High Field Saturation. Mobility Model

In device simulation, high field saturation mobility model is obtained by Canali model;

$$\mu_n = \frac{\mu_{n0}}{\left[1+\left[\frac{E\mu_{n0}}{\vartheta_{sat,n}}\right]^{\beta,n}\right]^{1/\beta,n}} \quad (2.3)$$

$$\mu_p = \frac{\mu_{p0}}{\left[1+\left[\frac{E\mu_{p0}}{\vartheta_{sat,p}}\right]^{\beta,p}\right]^{1/\beta,p}} \quad (2.4)$$

where $v_{sat} = v_{sat0}(\frac{T}{300})^{v_{sat,exp}}$ = 2.1 x 107 cm/s, and

$$\beta = \beta_o(\frac{T}{300})^{\beta_{exp}}$$

Temperature dependent bandgap model is designated as;

$$E_g(T)(eV) = \frac{E_g(300) + 2.206 \; x \; 10^{-2} \; T^2}{1 \; x \; 10^5 + T} \quad (2.5)$$

3. Device Structure

In current work, the structure was designed on the Sentaurus structure editor. The overall design of the device is shown in Figure 3.1 as a cross-sectional diagram.

The structure used for simulation has an active area of 9.3 x 10^{-4} cm^2. A 10 µm n-type layer along with doping concentration of 7 x $10^{15}/cm^3$ is used for drift region. The drift doping has a great impact in studying the forward and breakdown characteristics. The conduction current could be controlled by two p^+ gate regions that were defined with a width of 0.9 µm with a high doping concentration of 1 x $10^{18}/cm^3$. The separation between the two gates generates a channel of length 3.2 µm.

The channel width is more critical parameter and the values were selected to be 0.85, 1.05 and 1.25 µm (step 0.2 µm) with doping concentration of 7 x $10^{15}/cm^3$.

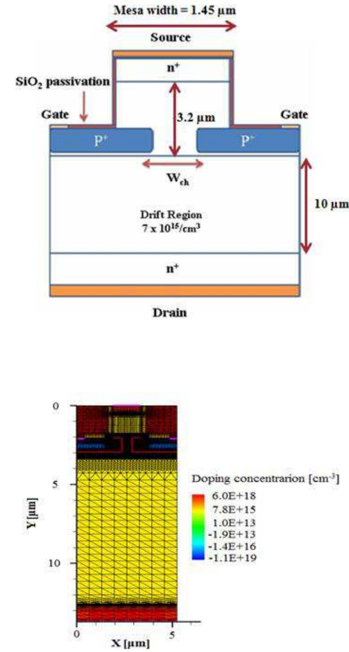


Figure 3.1: Cross. Sectional view of 4H-SiC VJFET and simulated 4H-SiC VJFET

2D numerical simulation of normally-off 4H-SiC VJFET was performed by varying different parameters including temperature (300 K - 600 K), channel width (0.85 µm, 1.05 µm and 1.25 µm) and gate voltage (2.5 V - 3.0 V) using TCAD numerical simulator. Various structural dimensions and doping concentrations are listed in table 3.1.

Table 3.1 : The Basic Parameters And Doping Profiles In Device Structure

Structure Region	Doping Type	Region Thickness	Doping concentration
Channel width	n^- type	0.85, 1.05 and 1.25 µm, (Step 0.2 µm)	7 x 10^{15} cm^{-3}
Channel length	n^- type	3.2 µm	7 x 10^{15} cm^{-3}
Drift layer	n^- type	10 µm	7 x 10^{15} cm^{-3}
Mesa width	--	1.45 µm	--
Source width	n^+ type	0.5 µm	1 x 10^{18} cm^{-3}
Drain width	n^+ type	1.0 µm	1 x 10^{18} cm^{-3}
Gate width	p^+ type	0.9 µm	1 x 10^{18} cm^{-3}

4. Results of Simulation and Discussion

Figures 4.1 (a) to (c) represent the simulated forward characteristics of VJFET at 300 K with different channel widths (0.85, 1.05 and 1.25 µm). While Figures 4.2 (a) to (c) represent the simulated forward characteristics of VJFET at 600 K with different channel widths (0.85, 1.05 and 1.25 µm). The positive gate voltage was applied in the range of 2.5 - 3.0 V with a regular step of 0.1V. It is evident from the characteristic curves that drain current becomes higher as gate voltage increases from 2.5 to 3.0 V for same value of drain voltage.

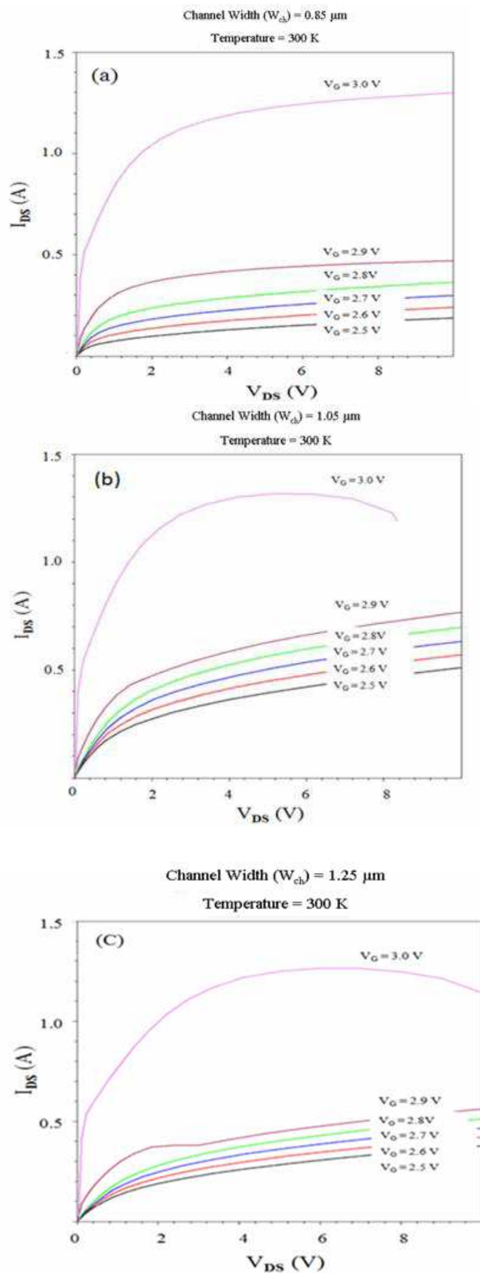


Figure 4.1: Forward conduction characteristics of the studied VJFET at 300 K

(a) W_{ch} = 0.85 µm
(b) W_{ch} = 1.05 µm
(c) W_{ch} = 1.25 µm

In figure 4.1 (c) when the applied V_{DS} is below 2 V, there is a sharp increase in drain to source current (I_{DS}) at 2.9 V of V_G. This rise in current is due to greater channel width, which is 1.25 µm and the appearance of a sub peak is showing this behavior. Above 2 V of V_{DS}, this rise in current gets smooth and regular due to saturation mode.

JFET is like voltage-controlled resistor. Basically, it is a semiconductor bar in which resistance can be. controlled by applying bias voltage to the gate. On-state resistance and saturation current were extracted at different temperatures, i.e. at 300, 400, 500 and 600 K.

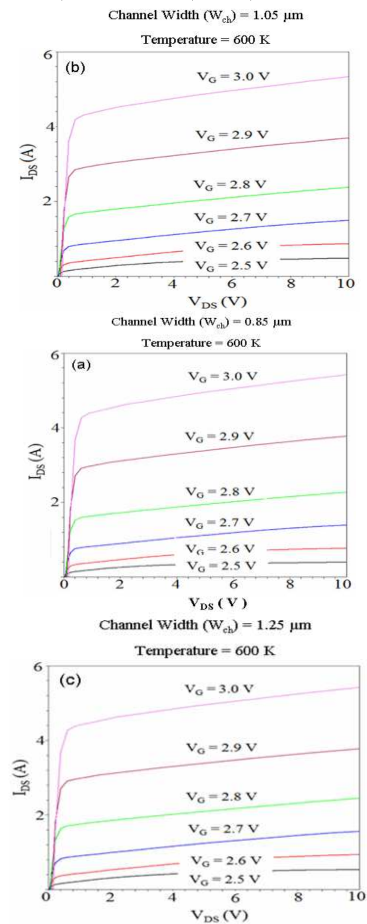


Figure 4.2: Forward conduction characteristics of
the studied VJFET at 600 K

(a) Wch = 0.85 µm
(b) (b) Wch = 1.05 µm
(c) (c) Wch = 1.25 µm

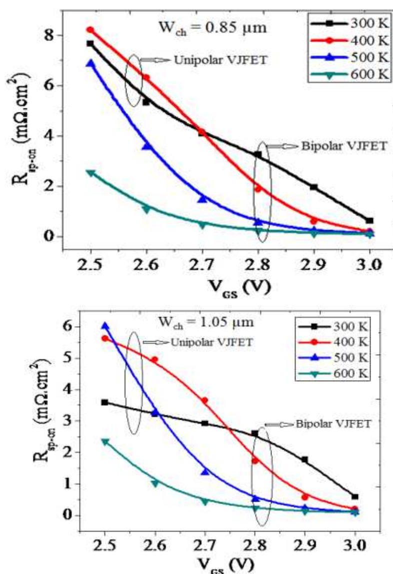
The on-resistance was extracted from the slope of the out-put transfer characteristic by gate bias ranging from 2.5 to 3.0 V with the regular steps of 0.1 V. In room-temperature. on-state drain-current measurements for 0.85 µm channel width at agate bias of 3.0 V, the

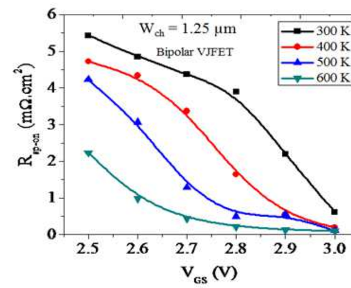
VJFET's drain current was 589 mA with a specific on-resistance of 0.631 mΩ.cm2. This was maximum on-resistance found at room temperature. In comparison of on-resistance at 2.9 V (Rsp-on = 2.01 mΩ.cm2), there is a 26.24 % fall in on-resistance at 3.0 V.

Figure 4.2 (a) illustrates the temperature dependence of on-resistance at channel width of 0.85 µm with gate voltage of 3 V. As it is clear from this figure, the temperature has significant effect on the on-resistance. On-resistance. decreases with increasing temperature.

The reduction in on-resistance can be due to the reduction in channel resistance with increasing high positive voltage along with high temperature. In these simulations, the minimum specific on-state resistance was observed as 0.101 mΩ.cm2 at 600 K, having VG = 3.0 V and Wch = 0.85 µm. Thus, it is indicated that by increasing the temperature from 300 to 600 K (keeping other parameters same), there is 83.9 % decrease in the specific on-resistance.

The variation of Rsp-on with VGS at temperatures 300, 400, 500 and 600 K are shown in figures 4.3 (a) to (c). The gate bias was varied from 2.5 to 3.0 V in steps of 0.1 V. These curves illustrate the comparison of unipolar and bipolar modes of operation in VJFET at different channel widths.





It is indicated from figure 4.3 (a) that for channel width of 0.85 µm, the structure exhibits unipolar behavior below 2.7 V of gate to source voltage at 300 and 400 K. While at $V_{GS} \geq 2.7$ V, it behaves like bipolar VJFET for entire temperature range (300 K– 600 K) because greater number of holes is injected into the channel region. It has been reported by Mihaila et al. that in order to get the required blocking ability, normally-off VJFETs should have either a narrow or lightly doped channel, which results in a high on-state resistance. For the purpose of compensation, they are operated in the bipolar mode [17].

In bipolar mode, gate junction injects minority carriers into the channel/drift region. In unipolar mode, the $R_{sp\text{-}on}$ is very high as compare to the specific resistance in bipolar mode. With the increase of 0.1V of VGS, i.e. from 2.9 to 3.0 V of VGS, there is 26.24 % decrease in specific resistance.

When the channel width is increased to a value of 1.05 µm, the unipolar behavior extends at temperatures of 300, 400 and 500 K below 2.7 V as shown in figure 4.3 (b). At VGS ≥ 2.7 V, the device becomes bipolar for all temperature values used in the simulation process. In bipolar mode, the device exhibits low specific resistance. With the increase of 0.1V of VGS, i.e. from 2.9 to 3.0 V of VGS, there is 25.52 % decrease in specific resistance. It is indicated from figure 4.3 (c), that at increased channel width of 1.25 µm, the bipolar mode of operation creates a sizeable impact. Here both types of charge carriers take part in the conduction process, irrespective of the temperature value. Specific on-resistance goes on decreasing with the increasing values of V_{GS}. With the increase of 0.1V of V_{GS}, i.e. from 2.9 V to 3.0 V of V_{GS}, there is 23.82 % decrease in specific resistance.The comparison of on-state resistance in current simulations with previously reported values is given in table 4.1. It is clearly indicated from table 4.1 that the design has a decent treaty with the experimental and theoretical data. The simulated specific on-resistance is equivalent to Rsp-on reported by Pezzimenti and Corte

(2012) [18] while it is 20 % higher than reported by Zhao et al. (2006) [19] and 37.9 % lower than reported by Sheng and Hu (2005) [20].

Table 4.1: Comparative analysis of on-resistance with previously reported values

Author (References)	Drift layer thickness (µm)	Drift layer doping (cm^{-3})	Specific on-resistance R_{sp-on} ($m\Omega.cm^2$)
(Pezzimenti and Corte, 2012)	7	3 x 10^{15}	2
(Veliadis et al., 2008)	12	5 x 10^{15}	5.5
(Zhao et al., 2006)	12	5 x 10^{15}	2.5
(Sheng and Hu, 2005)	8	3 x 10^{15}	3.24
(Zhao et al., 2004)	9.3	7 x 10^{15}	3.6
In current simulations	10	5 x 10^{15}	2.012

5. Conclusion

1229 V/ 5.43 A normally-off 4H-SiC VJFET has been intended and simulated using TCAD tools. The forward characteristics have been simulated with the impact of different parameters. including temperature, channel widths and gate voltages. The models and parameters. used for device simulation are physics based and mainly depend on the device geometry and doping. The optimized device with a channel width of 0.85 µm exhibited a specific on-resistance of 2.012 $m\Omega.cm^2$. The maximum saturation current 5.43A corresponding to low specific on-resistance of 0.101 $m\Omega.cm^2$ was observed at gate voltage of 3.0 V for 600 K. The unipolar on-resistance is 6.45 $m\Omega.cm^2$ with a gate bias of 2.6 V. Although operating in bipolar mode can decrease the on-state resistance, it leads to low current gain. The simulation results showed that the on-resistance decreases with increasing temperature.

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