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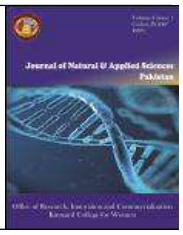

A PROPOSED CIRCUIT OF DARLINGTON PAIR BASED ON TRIPLE JFET CONFIGURATION

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Abstract

With passage of time, fast and efficient communication with minimum loss of signal is a much-desired aspect in modern technology. Knowledge of increasing demand of smaller, portable and modern forms of technology allows space for consideration of ways to produce devices that are at small size scale and efficient. This research is based on Darlington Transistors because of its rising demand and important features like high current and voltage gain. Proposition of JFET based triple Darlington topology lies in the sector of new researches done to widen the horizon of researchers of the day to help look beyond and capture the next step ahead and predict what next inventions may be. Unlike the conventional Darlington pair, the voltage gain of triple Darlington is considerably high and it also improves the poor response at high frequencies.

Keywords: JFET (junction field effect transistor),
BJT (bipolar junction transistor),
Darlington pair transistor,
Triple Darlington topology,
PSpice, current gain, voltage gain.

1. INTRODUCTION

Amplification is one of the most important phenomena in electronics. There are several methods to achieve amplification. The device used for this purpose in most cases is a transistor, used to amplify, control and generate electrical power signals. This research is focused on amplification using Darlington pair. A conventional Darlington pair is composed of two identical BJT transistors connected such that the emitter of first transistor is connected with the base of other transistor and collectors are joined together as shown in fig 1. This is done to get a larger current gain; so that a small amount of current from the input can be used to drive a larger load. Second transistor amplifies the current from first transistors. Thus, Darlington pair provides a large current gain which is equal to the product of current gains of the individual transistors.

Current gain of Darlington = $\beta_D = \beta_2$
β_1 (1)

The conventional Darlington pair has a major drawback that its frequency response exhibits poor response at large frequencies**.[ref]**The researchers have proposed a number of modifications in Darlington's configuration to overcome this problem**.[ref]**. In this research work, a new circuit is being presented which consists of three identical JFET (Junction Field Effect Transistors) to achieve better gain and frequency response. Furthermore different biasing resistances have been tries to get best possible voltage gain and current gain in the new proposed circuit. The proposed amplifier is well suited for the systems requiring high voltage gain and better response at high frequencies.T5his paper is described in four sections. First section gives the introduction of conventional Darlington pair and idea behind the proposed circuit. Section II provides the circuit description in detail. Section III contains the results and discussion and finally section IV concludes the proposed work.

II. CIRCUIT DESCRIPTION

Present work includes a comparison of two Darlington topologies; one with BJT Darlington transistor and the other JFET based triple Darlington topology. BJT Darlington is the reference circuit while the JFET triple Darlington is the proposed circuit. BJT Darlington pair transistor uses two BJTs in the reference circuit as depicted in Fig. 1.

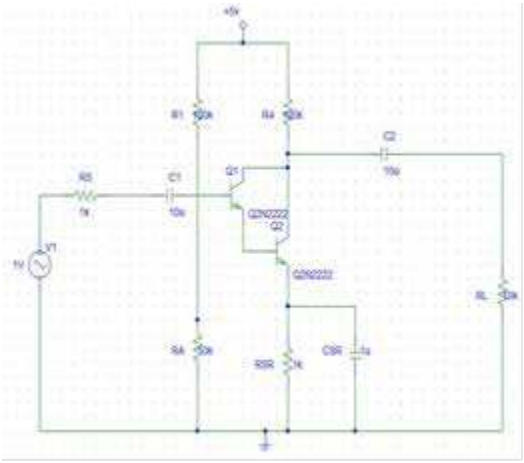

Fig. 1 Reference circuit of BJT Darlington pair

Whereas, as depicted in Fig. 2, the reference circuit that is Triple JFET based Darlington pair transistor contains not two but three identical JFETs. The three JFETs inflict the name Triple Darlington pair. Both circuits have bias resistances; R_A for reference and R_{AD} for proposed circuit.

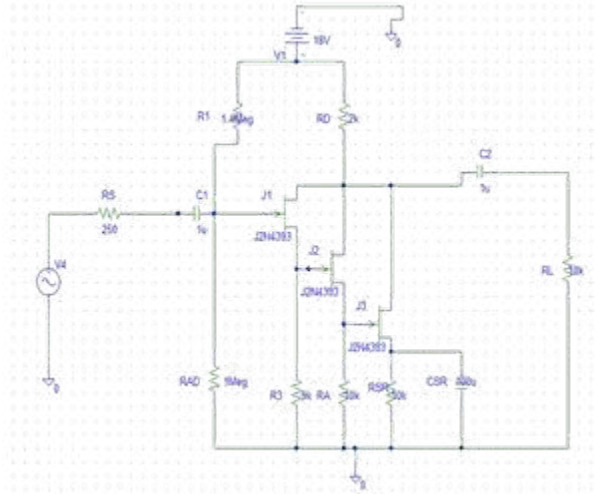

Fig. 2 Proposed circuit of Triple JFET Darlington pair

PSpice simulation is being performed to pursue this research. Circuit designs of these amplifier use potential divider biasing methodology. All the observations are made using AC analysis for both circuits. Table 1 enlists all components.

Table 1 Components detail of Circuits.

Components	**Description**	**Conventional Circuit**	**Proposed Circuit**
Q1, Q2:	NPN BJT	Q2N2222	-
J1,J2,J3	JFET	-	J2N4393
R_S	Source Resistance	1kΩ	250Ω
R_1	Biasing Resistance	100kΩ	1.4MΩ
R_4, R_D	Drain biasing Resistance	100kΩ	2kΩ
RSR	Source biasing Resistance	1kΩ	10kΩ
R_3	Additional biasing Resistance	-	9kΩ
R_L	Load Resistance	10kΩ	10kΩ
C_1	Coupling capacitor	10uF	1uF
C2	Coupling capacitor	10uF	1uF
CSR	Source bypass capacitor	1uF	100uF
Vcc	Biasing voltage	+5V	18V
V_1,V_4	AC input signal	1V	10mV

III. RESULTS AND DISCUSSIONS

Fig 3and fig 4 shows the voltage gain of conventional circuit and proposed circuit respectively. It can be seen clearly that the proposed circuit provides a considerable increase in voltage gain for a wide range of frequencies.

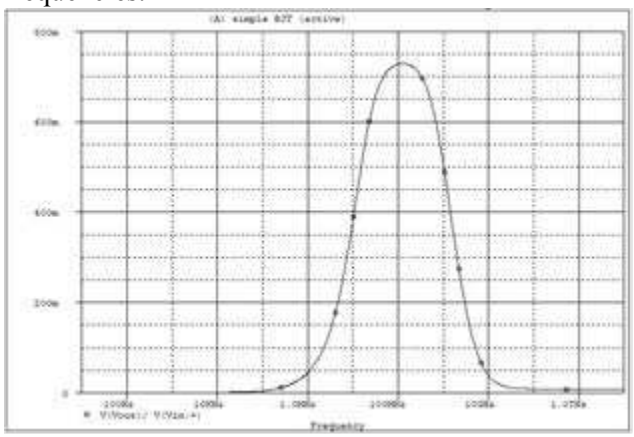

Fig. 3 Voltage gain of Conventional Darlington pair

At the input of 10mV provided at the AC voltage, the proposed Darlington pair transistor gives a voltage gain of about 10 while the frequency ranges from several Hz to several Mega Hz.

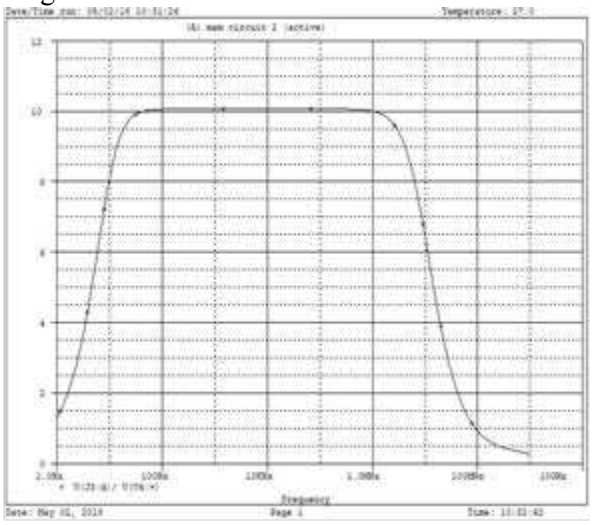

Fig. 4 Voltage gain of JFET triple Darlington pair

Current gain of proposed amplifier is also shown in Fig 5. The current gain gradually rises up to the value of 3k and then starts decaying from there and keeps decaying up till the range of Giga Hertz, in this case 120 GHz.

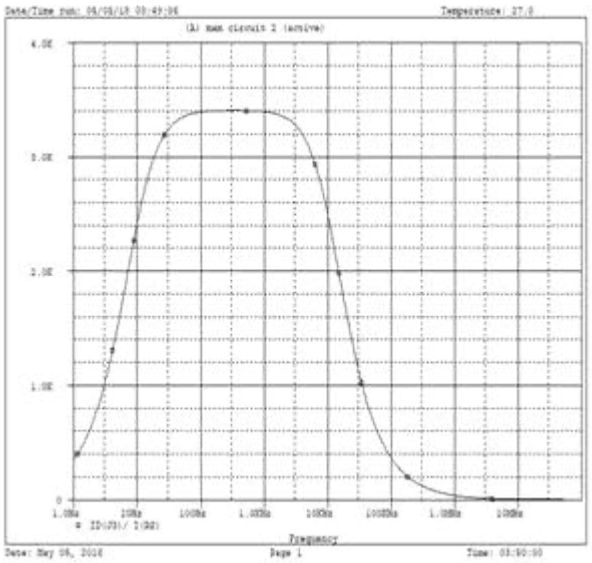

Fig. 5 Current gains of JFET triple Darlington pair

Bandwidth of the proposed circuit is 7.121391MHz which is appropriate for many electronic applications. Variations in values of biasing resistances R_{AD} for the proposed circuit give the response as per recorded in the table 2. Although, the best response recorded results from the biasing resistance of 1 Mega implemented in the circuit.

Table 2 Bias resistance R_{AD} variation response data

Values of R_{AD}	**Voltage gain of proposed circuit AVG**
1MΩ	10
100kΩ	7.2
10k Ω	6
1kΩ	4.96
100Ω	1.77

The pictorial representation of responses of variations in R_{AD} are given in fig. 6 to fig 9.

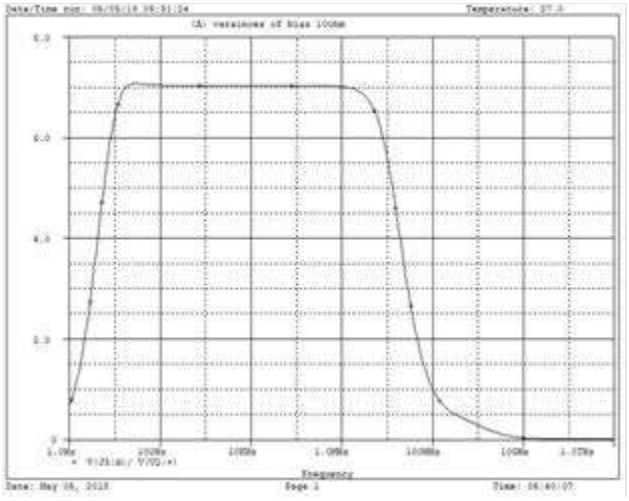

Fig. 6 Proposed circuit voltage gain response with R_{AD} at 100kΩ

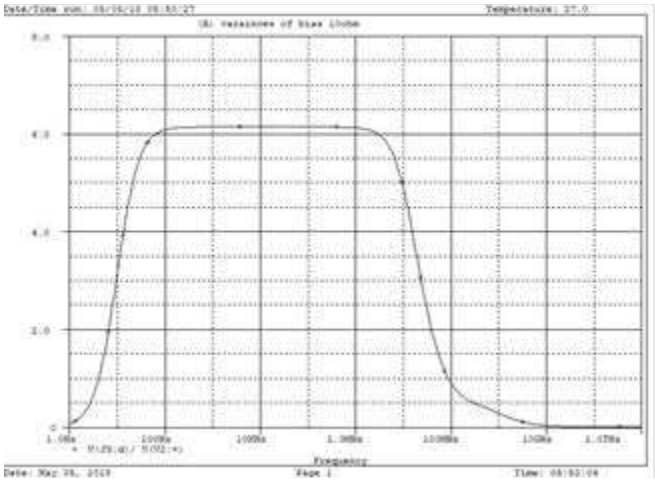

Fig. 7 Proposed circuit voltage gain response with R_{AD} at 10kΩ

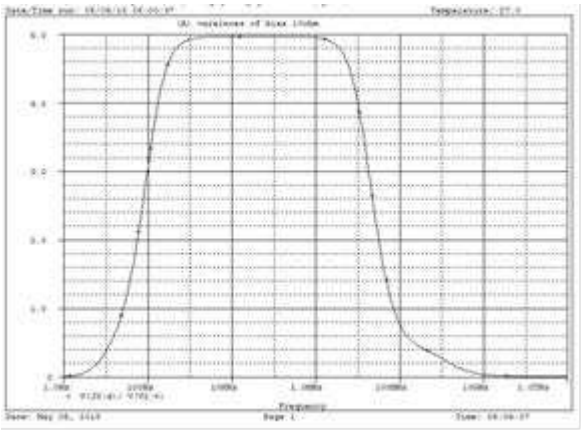

Fig. 8 Proposed circuit voltage gain response with R_{AD} at 1kΩ,

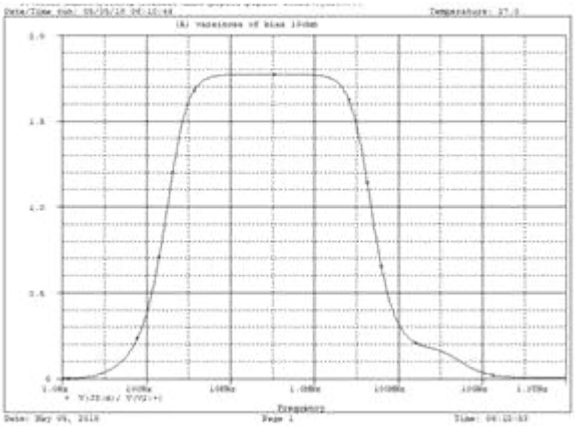

Fig. 9 Proposed circuit voltage gain response with RAD at 100Ω

IV. CONCLUSION

As compared with the reference circuit of standard BJT Darlington pair, the proposed triple JFET Darlington circuit gives much more efficient voltage gain of 10.15. Its current gain is 3k. Both gains are large for the input provided (10mV). The bandwidth for the proposed circuit is 7.121MHz which is better than BJT Darlington bandwidth. This supports the idea of practically putting into use the triple topology JFET based Darlington pair transistor. Increased biasing resistance RAD value improves the value of both voltage and current gain.

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